

**Listing of Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A method of manufacturing a microelectronic device, comprising:  
performing a first inspection of a device feature formed on a substrate during an intermediate stage of manufacture;  
cleaning the device feature after the first inspection; and  
performing a second inspection of the device feature after cleaning the device feature, wherein the first and second inspections are performed by a single inspection tool.
2. (Currently amended) A method of manufacturing a microelectronic device, comprising:  
performing a first inspection of a device feature formed on a substrate during an intermediate stage of manufacture;  
cleaning the device feature after the first inspection; and  
performing a second inspection of the device feature after cleaning the device feature, wherein the first inspection is performed by a first inspection tool and the second inspection is performed by a second inspection tool different than the first inspection tool.
3. (Canceled)
4. (Original) The method of claim 1 wherein at least one of the first and second inspections is performed by a scanning electron microscope (SEM).
5. (Original) The method of claim 1 wherein the cleaning comprises exposing the device feature to an oxygen containing plasma.
6. (Original) The method of claim 1 wherein the device feature comprises a first conductive layer located over a substrate, a buffer layer located over the first conductive layer, and a second conductive layer located over the buffer layer.
- 7 (Previously presented) A method of manufacturing a microelectronic device, comprising:

performing a first inspection of a device feature during an intermediate stage of manufacture;  
cleaning the device feature after the first inspection; and  
performing a second inspection of the device feature after cleaning the device feature, wherein the device feature is located in a production region of a wafer, the wafer further including a calibration region having a calibration feature located therein.

8. (Original) The method of claim 7 wherein the calibration feature comprises a first conductive layer located over the wafer, a buffer layer located over the first conductive layer, and a second conductive layer located over the buffer layer.

9. (Original) The method of claim 8 wherein the first conductive layer comprises AlCu, the second conductive layer comprises W, and the buffer layer comprises:  
a first TiN layer over the first conductive layer;  
an implanted Ti layer over the first TiN layer; and  
a second TiN layer over the implanted Ti layer.

Claims 10-22. (Canceled)

23. (Previously presented) The method of claim 2 wherein at least one of the first and second inspections is performed by a scanning electron microscope (SEM).

24. (Previously presented) The method of claim 2 wherein the cleaning comprises exposing the device feature to an oxygen containing plasma.

25. (Previously presented) The method of claim 2 wherein the device feature comprises a first conductive layer located over a substrate, a buffer layer located over the first conductive layer, and a second conductive layer located over the buffer layer.